CLAIMS

What is claimed is:

1. A memory architecture, comprising:

a main memory;

a level one cache, coupled to the main memory, for maintaining information; and

a level two cache, coupled between the main memory and the level one cache.

2. The memory architecture of claim 1, further including a graphics controller operative to send requests to the main memory.

3. The memory architecture of claim 1, wherein the level one cache comprises a plurality of cache blocks.

4. The memory architecture of claim 3, wherein the controller sends requests to at least a subset of the plurality of cache blocks, and the level two cache stores those requests that are sent to at least two of the plurality of cache blocks.

5. The memory architecture of claim 3, wherein the level two cache is coupled to at least one of the plurality of cache blocks of the level one cache.

6. A memory architecture for use in a graphics processor, comprising:

a level on cache including a plurality of cache blocks for maintaining information; and

a level two cache, coupled to at least one of the plurality of cache blocks, for maintaining information that is transmitted to at least one of the plurality of cache blocks, wherein information to be transmitted to a remaining one of the plurality of cache blocks is present within the level two cache.

7. The memory architecture of claim 6, further including a main memory, coupled to the level two cache, the main memory providing the information that is transmitted to at least one of the plurality of cache blocks.

8. The memory architecture of claim 7, wherein the memory structure is coupled to a graphics controller, the graphics controller operative to send requests to at least one of the plurality of cache blocks, wherein if the plurality of cache blocks cannot satisfy the request, the requested information is obtained from the main memory and the resulting information is stored in the level two cache before being provided to at least one of the plurality of cache blocks.

9. A graphics processing device, comprising:

a graphics controller operative to execute memory fetch instructions;

a main memory;

a level one cache including a plurality of cache blocks, coupled to the graphics controller, for maintaining appearance data; and

a level two cache, coupled between the main memory and the level one cache, operative to maintain data therein, wherein fetched information resulting from execution of overlapping memory fetch instructions is maintained within the level two cache such that subsequent requests for such fetched information is acquired from the level two cache.

10. The graphics processing device of claim 9, wherein if information relating to a memory request is not present in at least one of the plurality of cache blocks, a corresponding one of the plurality of cache blocks requests the information relating to the memory requests from the level two cache.

11. The graphics processing device of claim 10, wherein if the information relating to the memory requests is not present in the level two cache, such information is requested from the main memory block and such information is transmitted to the level two cache, such that subsequent requests for such information are obtained from the level two cache.